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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,395	12/15/2003	Grant W. McEwan	SC13108TP	6211
23125	7590	06/13/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			NGUYEN, THANH T	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/736,395	MCEWAN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-30 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/15/03</u> . | 6) <input type="checkbox"/> Other: ____.  |

## **DETAILED ACTION**

### ***Election/Restriction***

Applicant's election of Group I, claims 1-20 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 21-30 are withdrawn from further consideration by the examiner, 37 C.F.R. 1.142(b) as being drawn to a non-elected invention.

### ***Oath/Declaration***

The oath/declaration filed on 12/15/03 is acceptable.

### ***Information Disclosure Statement***

The Information Disclosure Statement filed on 12/15/03 has been considered.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

- (e) the invention was described in-
  - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
  - (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-6, 11-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Eissa (U.S. Patent No. 6,383,928).

Referring to figures 21-2h, Eissa teaches a method for preventing corrosion of metal surfaces of a semiconductor device during semiconductor processing, comprising:

Exposing a surface of a metal layer (118) of the semiconductor device;

Depositing and selectively bonding a sacrificial protective layer (120) overlying the exposed metal layer surface of the semiconductor device, wherein the sacrificial layer (120) protects the exposed surface from deleterious effects until subsequent processing of the semiconductor device (see figures 2d-2h); and

Subsequent processing of the semiconductor device, wherein the subsequent processing removes the sacrificial protective layer (see figure 2g-2h).

Regarding to claims 2, 14, the semiconductor device includes at least one of a portion of the semiconductor wafer and a semiconductor die (see figure 2a).

Regarding to claims 3, 15, the metal layer (118) includes a metal feature (112/114) of the semiconductor device (see figures 2b-2c).

Regarding to claims 4, 16, the exposed surface by itself is subject to deleterious effects in response to at least one of moisture containing ambient and an ambient conducive to causing corrosion (see col. 2, lines 45-65).

Regarding to claims 5, 17, exposing the surface can include a chemical mechanical polishing process (see col. 2, lines 45+).

Regarding to claims 6, 18, the deleterious effects include corrosion (see col. 2, lines 45-65).

Regarding to claims 11-13, forming another exposed metal layer comprising:

Exposing a surface of the another metal layer of the semiconductor device; depositing and selectively bonding another sacrificial protective layer overlying the another exposed metal layer surface of the semiconductor device, wherein the another sacrificial layer protects the another exposed surface from deleterious effects until subsequent processing of the semiconductor device; and subsequent processing of the semiconductor device, wherein the subsequent processing removes the another sacrificial protective layer (see col. 3, lines 53-56).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-9, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eissa (U.S. Patent No. 6,383928) applied to claims 1-6, 11-18 above in view of Avanzino et al. (U.S. Patent No. 6,350,687).

Eissa teaches a method for preventing corrosion of metal surfaces of a semiconductor device. However, the reference does not teach the deleterious effects include degraded semiconductor device reliability effects, and forming a sacrificial layer on the exposed metal layer surface by using a vapor corrosion inhibitor. Nevertheless, the process is well known in a semiconductor process.

Avanzino et al. teaches a process of preventing corrosion of metal surface of a semiconductor device by forming a copper layer (13) in the feature (opening) and treating (exposing) the surface of copper by using a vapor carrions inhibitor (see col. 5, lines 29-38, col. 6, lines 49-65) to form the sacrificial layer (40) on the exposed metal layer surface (see figure 4), and removing the sacrificial layer (40, see figures 4-5), wherein the sacrificial layer (40) has the thickness of 30-100A° (which greater than 1 monolayer, noted a nano layer varies from 5nm to 10 A°).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would the deleterious effects include degraded semiconductor device reliability effects, and forming a sacrificial layer on the exposed metal layer surface by using a vapor corrosion inhibitor in process of Eissa as taught by Avanzino et al. because the process would enables to form a thin controllable, uniform passivating layer (sacrificial layer) on an exposed surface of the metal.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (See **MPEP 203.08**).



Thanh Nguyen  
Patent Examiner  
Patent Examining Group 2800